AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Previously Presented) A testing architecture for automatic test equipment, comprising:

a signal source; and

a plurality of source/capture channels comprising one source/capture channel and remaining source/capture channels, the one source/capture channel being coupled to the signal source, the signal source being configured to provide a cancellation signal to reduce an amplitude of a signal received by the one source/capture channel, the one source/capture channel comprising:

a first combiner configured to receive a signal under test and a baseline signal and configured to provide a first combiner output signal; and

a second combiner configured to receive the first combiner output signal and the cancellation signal from the signal source, and configured to provide a second combiner output signal.

2. (Previously Presented) The architecture of claim 1 wherein the one source/capture channel further comprises a Digital-to-Analog Converter (DAC) configured to provide the baseline signal to the first combiner.

3. (Previously Presented) The architecture of claim 1, further comprising an external adjustment device coupled between the source and the plurality of source/capture channels.

4. (Previously Presented) The architecture of claim 1 wherein the one source/capture channel further comprises an Analog-to-Digital Converter (ADC) configured to receive the second combiner output signal.

5. (Cancelled)

6. (Currently Amended) The architecture of claim [[1]] 4 wherein the one source/capture channel further comprises:

an amplifier configured to receive the second combiner output signal and configured to provide an output signal to the ADC.

7. (Cancelled)

8. (Previously Presented) The architecture of claim 1 wherein the one source/capture channel comprises:

an amplifier configured to receive the second combiner output signal and configured to provide a residual signal to an Analog-to-Digital Converter (ADC).

9. (Previously Presented) The architecture of claim 4 wherein the one source/capture channel further comprises an amplifier configured to receive a signal from the signal source and configured to provide an output to the device under test.

10. (Previously Presented) The architecture of claim 4 wherein the one source/capture channel further comprises a Digital-to-Analog (DAC) configured to provide an output to a the device under test.

11. (Previously Presented) The architecture of claim 1 wherein the architecture is operable in a first mode wherein each channel of the plurality of source/capture channels is configured to perform a multiple capture, each channel configured substantially the same as the one source/capture channel.

12. (Previously Presented) The architecture of claim 1 wherein the architecture is operable in a second mode wherein the one source/capture channel is configured to perform a capture with signal cancellation.

13. (Previously Presented) The architecture of claim 1 wherein the architecture is operable in a third mode wherein each channel of the plurality of source/capture channels is configured to perform a capture with signal cancellation, each channel configured substantially the same as the one source/capture channel.

14. (Previously Presented) The architecture of claim 12 wherein in the second mode the remaining channels of the plurality of channels are configured to perform a multiple capture, each of the remaining channels comprising:

a first combiner configured to receive a signal under test and a baseline signal, and configured to provide a first combiner output signal;

a second combiner configured to receive the first combiner output signal and configured to provide a second combiner output signal; and

an amplifier configured to receive the second combiner output signal and configured to provide a residual signal to an ADC.

15. (Currently Amended) A reconfigurable testing architecture for automatic test equipment, comprising:

a signal source; and

a plurality of channels comprising one channel and remaining channels, the channels being each configurable into a plurality of modes, each of the modes providing a different level of precision from another of the modes,

wherein the one channel comprises:

a first combiner configured to receive a signal under test and a baseline signal, and configured to provide a first combiner output signal; and

a second combiner configured to receive the first combiner output signal and a cancellation signal from the signal source, and configured to provide a second combiner output signal.

16. (Previously Presented) The architecture of claim 15 wherein the plurality of modes includes a first mode wherein each channel is configured to perform a multiple capture, each channel being configured substantially the same as the one channel, the one channel further comprising:

an amplifier receiving said second combiner output signal and providing a residual signal to an Analog-to-Digital Converter (ADC).

17. (Previously Presented) The architecture of claim 15 wherein the plurality of modes includes a second mode wherein the one channel is configured to perform a capture with signal cancellation, the one channel further comprising:

an amplifier configured to receive the second combiner output signal and configured to provide a residual signal to an Analog-to-Digital Converter (ADC).

18. (Previously Presented) The architecture of claim 15 wherein the plurality of modes includes a third mode wherein each channel of the plurality of channels is configured to perform a capture with signal cancellation, the one channel further comprising:

an amplifier configured to receive the second combiner output signal and configured to provide a residual signal to an Analog-to-Digital Converter (ADC).

19. (Previously Presented) The architecture of claim 17 wherein in the second mode the remaining channels of the plurality of channels are configured to perform a multiple capture, each of the remaining channels comprising:

a first combiner configured to receive a signal under test and a baseline signal, and configured to provide a first combiner output signal;

a second combiner configured to receive the first combiner output signal and configured to provide a second combiner output signal; and

an amplifier configured to receive the second combiner output signal and configured to provide a residual signal to an Analog-to-Digital Converter (ADC).

20. (Currently Amended) A testing architecture for automatic test equipment, comprising:

a signal source; and

source/capture channels comprising one source/capture channel and remaining source/capture channels, the one source/capture channel being coupled to the signal source, the signal source being configured to provide a cancellation signal to reduce an amplitude of a signal received by the one source/capture channel, the one source/capture channel comprising:

a first combiner configured to receive a signal under test and a baseline signal and configured to provide a first combiner output signal;

a second combiner configured to receive the first combiner output signal and the cancellation signal from the signal source, and configured to provide a second combiner output signal;

an Analog-to-Digital Converter (ADC) configured to receive the second combiner output signal; and

a Digital-to-Analog Converter (DAC) configured to provide the baseline signal to the first combiner.

21. (Previously Presented) The architecture of claim 20, further comprising:

a first amplifier configured to receive the second combiner output signal and configured to provide an output signal to the ADC; and

a second amplifier configured to receive a signal from the signal source and configured to provide an output to the device under test.